AMENDMENTS TO THE SPECIFICATION

Please rewrite paragraph [0025] beginning at page 6, line 11 to read as follows.

--[0025] When it is determined that voltage across capacitor 20 has reached a value above the voltage set by first voltage reference 24, the output signal is shifted from the digital low to a digital high. As a result, the transmission gate 28 receives no signal due to the presence of inverter 30, thereby disconnecting first voltage reference from ~~capacitor~~ comparator 22. At the same time, transmission gate 32 is turned ON, thereby connecting second voltage reference source 34 to comparator 22. At this point, comparator 22 compares the voltage across capacitor 20 to the voltage provided by the second voltage reference 32. When the voltage across capacitor 20 reaches a voltage provided by the second voltage reference source 34, a low signal is outputted which in turn, turns off transmission gate 32 to cut off second voltage reference source 34 and turns on transmission gate 28 (due to the presence of inverter 30) thereby connecting first voltage reference source 24 to comparator 22. In addition, MOSFET 26 is turned off which allows capacitor 20 to charge up again. As a result, the output pattern shown in FIG. 2 is generated by the charging and discharging of capacitor 20. Therefore, as stated earlier, the minimum frequency may be set by selecting a proper resistance value for resistor 16.--